

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A differential transistor pair circuit having first and second resistive load elements coupled to collectors thereof, the improvement comprising:

an inductor coupled in series with each of the resistive load elements, such that the inductors are coupled to each other by mutual inductance to form a transformer having windings connected out of phase with said resistive load elements;

such that an inverted falling edge waveform at a node associated with the first resistive load element is coupled to a rising edge waveform at a node associated with the second resistive load element, substantially equalizing waveform rise and fall times.

2. (Previously presented) The differential transistor pair circuit of Claim 1 where the inductors are coupled out-of-phase to the collectors of the transistors.

3. (Currently amended) A differential circuit having a compound load, comprising: a differential pair of transistors having emitters coupled together; a resistive load resistor element coupled to a collector of each transistor to form first and second resistive load elements; and an inductor coupled in series with each of the load resistors, where the inductors are magnetically coupled together to form a transformer having windings connected out of phase with said resistive load elements; such that an inverted falling edge waveform at a node associated with the

first resistive load element is coupled to a rising edge waveform at a node associated with the second resistive load element, substantially equalizing waveform rise and fall times.

4. (Previously presented) The differential circuit of Claim 3 wherein the inductors are coupled out-of-phase to the collectors of the transistors.

5. (Original) The differential circuit of Claim 3 further comprises a common current source connected to the emitters of the transistors.

6. (Original) The differential circuit of Claim 3 wherein a differential signal of opposite polarity is applied to bases of the transistors.

7. (Original) The differential circuit of Claim 3 further comprises a buffer stage operable to reduce loading of the collectors of the transistors.

8. (Currently amended) A method for increasing bandwidth of a differential transistor pair circuit having first and second resistive load elements coupled to collectors thereof, comprising:

connecting an inductor in series with each of the resistive load elements to form a transformer having windings connected out of phase with said resistive load elements; and  
~~magnetically coupling the inductors together~~

coupling an inverted falling edge waveform at a node associated with the first resistive load element to a rising edge waveform at a node associated with the second resistive load element to substantially equalize waveform rise and fall times.

9. (Currently amended) A differential circuit having a compound load, comprising:  
a differential pair of transistors having emitters coupled together;  
a load resistor coupled to a collector of each transistor to form first and second load resistors; and

a transformer having a pair of inductors coupled to each other by mutual inductance and each coupled in series with one of the load resistors to form a transformer having windings connected out of phase with said load resistors;

such that an inverted falling edge waveform at a node associated with the first load resistor is coupled to a rising edge waveform at a node associated with the second load resistor, substantially equalizing waveform rise and fall times.

10. (Previously presented) The differential circuit of Claim 9 wherein the inductors are coupled out-of-phase to the collectors of the transistors.

11. (Previously presented) The differential circuit of Claim 9 further comprises a common current source connected to the emitters of the transistors.

12. (Previously presented) The differential circuit of Claim 9 wherein a differential signal of opposite polarity is applied to bases of the transistors.

13. (Previously presented) The differential circuit of Claim 9 further comprises a buffer stage operable to reduce loading of the collectors of the transistors.